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[TITLE OF THE INVENTION]

Semiconductor Device and Method of Manufacturing the Same

[ABSTRACT]

[Problem to be Solved]

To stably form a gate insulating film having two or more kinds of film thickness on the same substrate with higher controllability.

[SOLUTION]

A silicon nitride film 7 is formed first in the first thickness on the entire surface of an element region and the silicon nitride film is removed next only from the region where the silicon nitride film in the second thickness is formed.

Thereafter, a silicon oxide film is formed to the entire surface again with a method in which the oxidation and nitridation are combined. In this case, since the silicon nitride film portion has the higher anti-oxidation property, film thickness does not increase and is maintained at the initial film thickness, while a silicon oxide film 11 in the second thickness is formed to the other portion. As described above, since the film is formed with the single process in the two kinds of thickness, two kinds of film thickness may be formed stably with higher controllability.

[CLAIMS]

[Claim 1]

A semiconductor device allowing formation of a plurality of field effect transistors including gate insulating films of different kinds of film thickness on the same substrate, wherein the thinnest gate insulating film is formed with inclusion of an anti-oxidation film which is placed in direct contact with a silicon substrate and the gate insulating films of the other film thickness are formed with inclusion of a silicon oxide film or a silicon acid nitride film.

[Claim 2]

The semiconductor device according to claim 1, wherein each gate insulating film includes, at an upper layer portion thereof, a film having a dielectric constant which is higher than that of silicon nitride.

[Claim 3]

The semiconductor device according to claim 1 or 2, wherein said anti-oxidation film is a silicon nitride film.

[Claim 4]

The semiconductor device according to claim 3, wherein nitrogen content of the silicon nitride film is 12 to 57 atom%.

[Claim 5]

The semiconductor device according to any of claims 1 to 4, wherein nitrogen content of the silicon oxide film or silicon acid nitride film is 5 atom% or less.

[Claim 6]

A method of manufacturing a semiconductor device including a field effect transistor having gate insulating films of different kinds of thickness within a plurality of element regions, comprising the steps of:

(1) forming respectively thin anti-oxidation films of the first thickness within a plurality of element regions;

(2) removing, by the etching process, the anti-oxidation films in the regions except for the element region where a thin gate insulating film is formed;

(3) forming a thick silicon oxide film or a thick silicon acid nitride film which is thicker than the film of the first thickness on the element region other than the region where the anti-oxidation film is formed with the oxidation or acid nitridation using the anti-oxidation film as the oxidation or acid nitridation mask;

(4) forming gate electrodes to a plurality of element regions by depositing a conductive film and then patterning the same conductive film; and

(5) forming source and drain regions respectively within a plurality of element regions.

[Claim 7]

The method of manufacturing semiconductor device according to claim 6 including the field effect transistor in which three or more element regions are provided and a gate

insulating film of an intermediate thickness between the gate insulating film of the first thickness and the gate insulating film of the maximum thickness is also provided, wherein a step (i) of removing, by the etching process, the gate insulating film on the region where the gate insulating film of the intermediate thickness is formed and a step (ii) of forming the silicon nitride film or silicon acid nitride film which is thicker than the first thickness on the element regions other than that where the anti-oxidation film is formed by executing oxidation or acid nitridation using the anti-oxidation film as the oxidation or acid nitridation mask are inserted once or a plurality of times between the step (3) and step (4) described above.

[Claim 8]

The method of manufacturing semiconductor device according to claim 6 or 7, wherein a step of depositing a film of the dielectric constant which is higher than that of silicon nitride is inserted between the step (3) and the step (4) or between the step (ii) and the step (4).

[Claim 9]

The method of manufacturing semiconductor device according to any of claims 6 to 8, wherein the anti-oxidation film formed in the step (1) is the silicon nitride film including nitrogen content of 12 to 57 atom% and the oxidation

or acid nitridation in the step (ii) is performed under the temperature of 800°C or less.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical field of the Invention]

The present invention relates to a semiconductor device including an insulated gate type field effect transistor (hereinafter, referred to as MOSFET with inclusion of the same transistor including the gate insulating film other than an oxide film) and more specifically to a semiconductor device including MOSFETs including the gate insulating films of different kinds of thickness on the same substrate and to a method of manufacturing the same transistor.

[0002]

[Prior Art]

When it is required for loading of circuits to mix the circuits in different functions and voltages used such as DRAM or SRAM and logic circuit, and CPU portion in the logic circuit and input and output interface portions, etc., it is also required to form, on the same substrate, the MOSFETs which have been designed in different structures. In this case, since the voltage applied to a gate electrode in accordance with application of MOSFET is often different and drive capability required in accordance with application is also often different, it is required to form the MOSFETs on the same

substrate with difference in thickness of the gate insulating film. However, formation in good reproducibility and high accuracy of extremely thin gate insulating films in different kinds of thickness is exactly difficult and this difficulty is just an important technical problem for manufacture of LSI having different kinds of functions.

[0003]

Figs. 6A to 6D are cross-sectional views in the manufacturing steps for illustrating the conventional art in which the MOSFETs including the gate insulating films of different kinds of thickness. First, an element isolating and insulating film 41 is formed with a silicon oxide film (SiO_2) on a well 40. Next, a gate insulating film 39 consisting of a silicon oxide film is formed with thermal oxidation process to the entire surface of an element region [Fig. 6(a)]. Next, only the gate insulating film in the region to form a thin gate insulating film is removed with the etching process using a photoresist film 42 as the mask [Fig. 6(b)]. Moreover, when the thermal oxidation is conducted to the entire surface of element region, a thin gate insulating film 43 is formed in the region where the gate insulating film is removed and a thick gate insulating film 44 is further formed to the masked region because the oxidation has also been performed. As a result, thin gate insulating film and thick gate insulating film in the desired two kinds of thickness have been formed [Fig. 6(c)].

Moreover, a gate electrode 45 of three-layer structure of polysilicon, tungsten nitride, and tungsten (W/WN/Poly. Si) is formed on the thin gate insulating film and thick gate insulating film. Finally, the source and drain region 46 is formed [Fig. 6(d)].

[0004]

[Problem to be Solved by the Invention]

However, it is difficult for this method in which the etching and re-oxidation processes are utilized to stably obtain the insulating films including large difference in film thickness as in the case that a transistor including a gate insulating film thinner than 3 nm as a result of ultra-fine processes and a transistor including a gate insulating film as thick as about 6 nm are formed on the same wafer. Moreover, when the gate insulating films of three kinds of film thickness are formed on the same wafer, a problem is generated in which controllability of film thickness is deteriorated.

[0005]

In addition, when the field effect transistors including gate insulating films having large difference in film thickness are formed on the same wafer, following problem is generated. That is, when the gate insulating film thickness is reduced in order to enhance the drive capability, a boron penetration problem becomes distinctive in a p-channel MOSFET (hereinafter, described to as pMOSFET). Therefore, it is

required to introduce nitrogen into the gate insulating film. However, when nitrogen is introduced into the gate insulating film, controllability of etching process and re-oxidation becomes worse than that when the gate insulating film to which nitrogen is not introduced is used and it becomes more difficult to stably form the gate insulating films of different kinds of thickness.

[0006]

A nitrogen-added gate insulating film or a gate nitride film is used as a measure for preventing cutting-through of boron in the pMOSFET wherein the thinner gate insulating film is provided in order to enhance the drive capability as described above. Meanwhile, use of a gate oxide film which does not allow flow of a gate leak current and ensures higher breakdown voltage of insulating film and long-term reliability is more suitable in the transistor where the thick gate insulating film is used. Hence, in these years, it has been attempted to use a film having a higher dielectric constant such as Ta_2O_5 and TiO_2 as the gate insulating film, but since these films having a higher dielectric constant have been formed with a film forming method which results in the controllability of film thickness which is worse than that of the thermal oxidation and nitridation, it is truly difficult to form the gate insulating films of different kinds of thickness using the high dielectric constant film.

[0007]

The principal object of the present invention is therefore to provide a semiconductor device comprising a MOSFET which includes, on the same substrate, the gate insulating films of two or more kinds of stable thickness. Moreover, the other object of the present invention is to form the gate insulating films of different kinds of thickness with good controllability of film thickness even when a high dielectric constant film is used.

[0008]

[Means for Solving the Problems]

In view of attaining the objects described above, according an aspect of the present invention, there is provided a semiconductor device in which a plurality of field effect transistors including the gate insulating films of different kinds of thickness are formed on the same substrate, wherein the thinnest gate insulating film is formed with inclusion of anti-oxidation film which is placed in direct constant with a silicon substrate and the gate insulating films of the other thickness is formed with inclusion of a silicon oxide film or a silicon acid nitride film.

[0009]

Moreover, in view of attaining the objects described above, according to another aspect of the present invention, there is provided a method of manufacturing semiconductor

device which includes field effect transistors including the gate insulating films of different kinds of thickness within a plurality element regions, comprising the steps of:

(1) forming respectively thin anti-oxidation films of the first thickness within a plurality of element regions;

(2) removing, by the etching process, the anti-oxidation films in the regions except for the element region where a thin gate insulating film is formed;

(3) forming a thick silicon oxide film or a thick silicon acid nitride film which is thicker than the film of the first thickness on the element region other than the region where the anti-oxidation film is formed with the oxidation or acid nitridation using the anti-oxidation film as the oxidation or acid nitridation mask;

(4) forming gate electrodes to a plurality of element regions by depositing a conductive film and then patterning the same conductive film; and

(5) forming source and drain regions respectively within a plurality of element regions.

[0010]

[Operation]

The semiconductor device of the present invention is characterized in that an anti-oxidation film such as silicon nitride film is used as a thin gate insulating film and a thick gate insulating film is formed of a silicon oxide film or a

silicon acid nitride film of low nitrogen concentration. Accordingly, the thin gate insulating film can control the cutting-through of boron and can obtain excellent drive capability. The silicon nitride film has the dielectric constant which is higher than that of the silicon oxide film. Therefore, the gate insulating film can be designed in the thickness which is thicker than the silicon oxide film when it is required to obtain the identical current drive capability. As a result, a gate leak current such as a tunnel current or the like can be controlled. Moreover, reliability for dielectric strength and deterioration by aging can be improved and the gate leak current characteristic can also be improved by using a silicon oxide film or a silicon acid nitride film of low nitrogen concentration for the thick gate insulating film.

[0011]

The method of forming the gate insulating film of the present invention is capable of forming the films of different kinds of thickness with single film forming process in excellent controllability for film thickness because the anti-oxidation film ensuring higher anti-oxidation property is formed first as the thin gate insulating film and only the thick gate insulating film portion is formed with the silicon oxidation process by utilizing the intensive anti-oxidation property of the thin gate insulating film.

[0012]

[PROFILES OF EMBODIMENT OF THE PRESENT INVENTION]

Next, the profiles of embodiment of the present invention will be described with reference to the accompanying drawings. Fig. 1 is a cross-sectional view illustrating a first profile of the embodiment of the present invention. As illustrated in Fig. 1, a well 1 is isolated to a plurality of element regions with an element isolating and insulating film 3. In the semiconductor device of this embodiment, a thin gate insulating film 6 is formed using an anti-oxidation film such as a silicon nitride film (Si_3N_4) or the like, while a thick gate insulating film 4 is formed of a silicon oxide film or of a silicon acid nitride film of low nitrogen concentration. Moreover, a gate electrode 5 of the three-layer structure of polysilicon, tungsten nitride and tungsten is formed over the thin gate insulating film 6 and thick gate insulating film 4, while source and drain regions 2 are formed in the well 2 sandwiching the gate electrode 5.

[0013]

Figs. 2(a) to 2(d) are cross-sectional views in the manufacturing steps illustrating a manufacturing method of semiconductor device of the first profile of the embodiment of the present invention. After the well 8 is isolated into a plurality of element regions by forming the element isolating and insulating film 9 over the well 8, the thin gate insulating

film 7 having higher anti-oxidation property is formed over each element region [Fig. 2(a)]. The gate insulating film 7 formed with this step is required to have the higher anti-oxidation property. Here, higher anti-oxidation property means the function that film thickness is never changed in the subsequent thermal oxidation step and thermal acid nitridation. For this purpose, for example, when the gate insulating film 7 is formed with a silicon nitride film, nitrogen concentration is controlled to enter the range of 12 to 57 atom%. Next, a photoresist film 10 is formed over the region to form the thin gate insulating film and the gate insulating film 7 is removed from the region to form the thick gate insulating film with the wet etching process using the photoresist film 10 as a mask [Fig. 2(b)]. Moreover, the thick gate insulating film 11 is formed with the oxidation process or with a method combining the oxidation and nitridation [Fig. 2(c)]. In this step, the thermal oxidation or thermal nitridation is performed under the temperature condition of 800°C or lower in which the thickness of thin gate insulating film 7 is never changed. Moreover, nitrogen content atom% is controlled to 5 or less in order to acquire the formed film quality of oxide film or acid nitride film. Finally, the gate electrode 12 is formed over the gate insulating film and the source and drain region 13 is formed within the silicon substrate [Fig. 2(d)].

[0014]

Fig. 3 is a cross-sectional view illustrating a second profile of embodiment of the present invention. As illustrated in Fig. 3, the source and drain region 18 and the element isolating region 19 are formed over the surface region of the well 17, while the gate insulating films 15, 20 and the gate electrode 14 are formed over the well. Difference from the first embodiment illustrated in Fig. 1 of the present invention is that a high dielectric constant film 16 formed of tantalum oxide (Ta_2O_5) is formed over the thin anti-oxidation film 15a and thick oxide film 20a and a thin laminated gate electrode 15 and a thick laminated gate electrode 20 are formed in the respective regions. When a high dielectric constant film is used for a gate insulating film, it has been difficult to form the gate insulating films of different kinds of thickness because the processes of high dielectric constant film has also been difficult. According to the present invention, the gate insulating films of different kinds of thickness can be formed by changing film thickness of the thin anti-oxidation film 15a and thick oxide film 20a without change in the thickness of the high dielectric constant film 16. Moreover, the thin anti-oxidation film 15a and thick gate insulating film 20a are also used as a lower-layer barrier film of the high dielectric constant film 16.

[0015]

Fig. 4 shows cross-sectional views of the manufacturing steps illustrating a manufacturing method of the second profile of embodiment of the present invention. After the element region is segmented by forming the element isolating and insulating film 23 over the well 22, the anti-oxidation film 21a is formed in each element region [Fig. 4(a)]. Next, the region to form the thin gate insulating film is covered with the photoresist film 24 and the anti-oxidation film 21a is removed from the region to form the thick gate insulating film with the wet etching process using the photoresist film 24 as a mask [Fig. 4(b)]. Moreover, the thick oxide film 25a is formed with the oxidation process or the method combining the oxidation and nitridation processes [Fig. 4(c)]. Next, the high dielectric constant film 26 is laminated over the entire surface of substrate using tantalum oxide in order to form the thin laminated gate electrode 21 and thick laminated gate electrode 25 [Fig. 4(d)]. Thereafter, a laminated film of W/WN/poly-Si or the like is deposited over the high dielectric constant film 26 and this laminated film is then patterned to form the gate electrode 27 and also form the source and drain region 28 over the well 22 [Fig. 4(e)].

[0016]

Fig. 5 shows cross-sectional views of the manufacturing steps illustrating a manufacturing method of a third profile of embodiment of the present invention. In the first and second

profiles of embodiment of the present invention described above, the gate insulating films of two kinds of thickness have been formed, but in this profile of embodiment, three gate insulating films of three kinds of thickness are formed. After the element isolating and insulating film 31 is formed over the surface of the well 30 and this film 31 is isolated into a plurality of element regions, the thin anti-oxidation gate insulating film 29 is formed in each element region [Fig. 5(a)]. Next, the region to form the thin gate insulating film is covered with the photoresist film 32 and the gate insulating film 29 is removed from the region to form the thick gate insulating film and the gate insulating of an intermediate thickness with the wet etching process using the photoresist film 32 as a mask [Fig. 5(b)]. Next, the gate insulating film 33 is formed with the oxidation process or the method combining the oxidation and nitridation processes [Fig. 5(c)]. Thereafter, the region to form the thin gate insulating film and the region to form the thick gate insulating film are covered with the photoresist film 34 and the gate insulating film 33 is removed with the wet etching process from the region to form the gate insulating film of the intermediate thickness using the photoresist film 34 as a mask [Fig. 5(d)]. Moreover, the gate insulating film 36 of the intermediate thickness is formed with the oxidation process or the method combining the oxidation and nitridation processes. In this timing, the gate

insulating film 33 is further oxidized or nitrided, although thickness of the thin gate insulating film is not changed. As a result, the thick gate insulating film 35 is formed [Fig. 5(e)]. Finally, a conductive film is formed over the gate insulating film and this conductive film is patterned to form a gate electrode 37 and to form the source and drain region 38 within the well 30 [Fig. 5(f)].

[0017]

[Embodiments]

The first embodiment will be described with reference to Fig. 2. After the element isolating and insulating film 9 consisting of silicon oxide film is formed in the thickness of 350 nm with the shallow-trench method in order to isolate the element regions, a silicon nitride film in the thickness of 2 nm which will become the thin gate insulating film 7 is formed through the thermal nitridation under 1100°C using high purity nitrogen with residual oxygen of 0.1 ppm or less [Fig. 2(a)]. A silicon nitride film (thin gate insulating film 7) is then removed from the region to form the thick gate insulating film using hot phosphoric acid with the photoresist film 10 used as a mask [Fig. 2(b)]. Next, a silicon oxide film is formed through growth in thickness of 4 nm with the thermal oxidation of the thick gate insulating film 11 under 780°C using dry oxygen [Fig. 2(c)]. The laminated film of polysilicon, tungsten nitride and tungsten is deposited in the total thickness of 35 nm and this

film is patterned to form the gate electrode 12. Finally, the source and drain region 13 is formed by implantation of phosphorus (P) ion [Fig. 2(d)].

[0018]

According to the manufacturing method of this embodiment, the thin gate insulating film 7 has extensive anti-oxidation property and therefore it maintains the initially determined thickness without increase in the thickness during the thermal oxidation process. Moreover, the thick gate insulating film 11 is formed with single oxidation process. Since the thin gate insulating film and thick gate insulating film are formed respectively with single forming process, both films can be formed in the stable thickness. Moreover, since the thin gate insulating film 7 is formed of silicon nitride film, this film can provide the effect of suppressing penetration of boron of the pMOSFET. In addition, since the thick gate insulating film 11 is formed of silicon oxide film, this film ensures higher reliability of dielectric strength and deterioration by aging. Further, the manufacturing method of this embodiment can provide a merit that when the gate insulating film 7 is removed with phosphoric acid [Fig. 2(b)], reduction in the element isolating and insulating film 9 can be controlled because the gate insulating film 7 is formed of the silicon nitride film, while the element

isolating and insulating film 9 is formed of the silicon oxide film.

[0019]

Next, the second embodiment will be described with reference to Figs. 4A to 4E. The element isolating and insulating film 23 is formed of a silicon oxide film in the thickness of 350 nm, while the silicon nitride film which will become the anti-oxidation film 21a is formed in the thickness of 2 nm with direct nitridation under 1100°C using the high purity ammonium gas [Fig. 4(a)]. Using the photoresist film 24 as a mask, the anti-oxidation film 21a in the region to form the thick gate insulating film is removed with the wet etching process using the hot phosphoric acid [Fig. 4(b)]. The silicon acid nitride film which will become the thick oxide film 25a is formed in the thickness of 4 nm with thermal acid nitridation under 780°C using a mixed gas of oxygen of 80 mol% and ammonium of 20 mol% [Fig. 4(c)]. The Ta_2O_5 film in the thickness of 4 nm which will become the high dielectric constant film 26 is deposited with the CVD method and the thin gate insulating film 21 and thick gate insulating film 25 are formed through the heat treatment for compensating for shortage of oxygen in the Ta_2O_5 film [Fig. 4(d)]. Next, the laminated film of polysilicon, tungsten nitride, and tungsten is deposited in the total thickness of 35 nm and this film is patterned to form the gate

electrode 27. Finally, the source and drain region 28 is formed through implantation of the phosphor (P) ion [Fig. 4(e)].

[0020]

Next, the third embodiment of the present invention will be described with reference to Figs. 5(a) to 5(f). With the shallow-trench method, the element isolating and insulating film 31 is formed with the silicon oxide film in the thickness of 350 nm and the silicon nitride film which will become the thin gate insulating film is formed in the thickness of 2 nm with the direct nitridation method under 1100°C using the high purity ammonium gas [Fig. 5(a)]. The region to form the thin gate insulating film is covered with the photoresist film 32 and the silicon nitride film (29) is removed, with the wet etching process using the hot phosphoric acid, from the region to form the thick gate insulating film and the gate insulating film of the intermediate thickness using the photoresist film as a mask [Fig. 5(b)]. Next, the silicon oxide film which will become the gate insulating film 33 is formed in the thickness of 3 nm with the steam oxidation under 780°C [Fig. 5(c)]. Next, the region to form the thin gate insulating film and the region to form the thick gate insulating film are covered with the photoresist film 34 and the gate insulating film 33 in the region to form the gate insulating film of the intermediate thickness is removed with the wet etching process using the buffered phosphoric acid with the photoresist film 34 used as

a mask [Fig. 5(d)]. Thereafter, the silicon oxide film which will become the gate insulating film of the intermediate thickness is formed in the thickness of 4 nm with the steam oxidation method under 780°C [Fig. 5(e)]. In this timing, the gate insulating film 33 is further oxidized to form thereby the thick gate insulating film 35 as the silicon oxide film in the thickness of 6 nm. Thereafter, with the method similar to that in the preceding embodiment, the gate electrode 38 and source and drain region 38 are formed [Fig. 5(f)].

[0021]

In the case where the gate insulating films of three different kinds of thickness are formed over the same wafer, it is difficult to control the film thickness with higher accuracy. In this embodiment, the thin gate insulating film 29 is formed of silicon nitride film, while the thick gate insulating film 35 and the gate insulating film 36 of the intermediate thickness are formed of silicon oxide film. When the gate insulating film is thick, stable silicon oxide films of different kinds of thickness can be formed with the etching process and re-oxidation process. Moreover, since the thin gate insulating film 29 is the anti-oxidation silicon nitride film, film thickness does not change even after the two times of thermal oxidation and the effect for suppressing penetration of boron of the pMOSFET can be attained. In addition, since the thick gate insulating film 35 and the gate insulating film

36 of the intermediate thickness are silicon oxide films, higher reliability can be ensured for dielectric strength and deterioration by aging.

[0022]

The preferred embodiments and profiles of embodiment have been described above. However, the present invention is not restricted by these profiles of embodiment and the preferred embodiments and allows adequate changes or modifications within the scope not departing from the subject matters of the claims thereof. For example, the gate electrodes of three different kinds of thickness including the high dielectric constant film can be formed by combining the second profile and the third profile of embodiment. Moreover, it is also possible to form the gate insulating films of four or more different kinds of thickness may be formed by expanding the manufacturing method of the third profile of the embodiment.

[0023]

[Effects of the Invention]

As described above, the semiconductor device of the present invention is capable of forming the gate insulating films of two or more kinds of stable thickness on the same substrate by forming the thin gate insulating film with the anti-oxidation film such as silicon nitride film and the thick gate insulating film with the silicon oxide film or silicon acid nitride film. Moreover, the semiconductor device of the

present invention can provide the effect of controlling cutting-through of boron of the pMOSFET because the thin gate insulating film is the silicon nitride film. In addition, the silicon nitride film can be designed as the thick film and can control a gate leak current due to the tunnel, when it is required to attain the identical current drive capability because this film has the dielectric constant which is higher than that of the silicon oxide film. Further, since the thick gate insulating film is basically the silicon oxide film, this film ensures higher reliability for dielectric strength and deterioration by aging. Moreover, when the thin gate insulating film is removed with phosphoric acid, reduction of element isolating and insulating film can be controlled because the element isolating and insulating film is formed of silicon oxide film. Furthermore, according to the embodiment wherein high dielectric constant films are laminated over the insulating films of different kinds of thickness, the gate insulating films of different kinds of thickness can be formed easily using the high dielectric constant films and a lower layer barrier film of the high dielectric constant film can also be formed simultaneously.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

A cross-sectional view of a semiconductor device for describing a first profile of embodiments of the present invention.

[Fig. 2]

Cross-sectional views of manufacturing steps of the first profile of embodiments and a first embodiment of the present invention.

[Fig. 3]

A cross-sectional view of the semiconductor device for describing a second profile of embodiments of the present invention.

[Fig. 4]

Cross-sectional views of manufacturing steps of the second profile of embodiments and a second embodiment of the present invention.

[Fig. 5]

Cross-sectional views of manufacturing steps of a third profile of embodiments and a third embodiment of the present invention of the present invention.

[Fig. 6]

Cross-sectional views of manufacturing steps of the conventional art.

[DESCRIPTION OF REFERENCE NUMERALS]

1, 8, 17, 22, 30, 40: Well;

2, 13, 18, 28, 38, 46: Source and drain region;

3, 9, 19, 23, 31, 41: Element isolating and insulating film;

4, 11, 35, 44: Thick gate insulating film;

5, 12, 14, 27, 37, 45: Gate electrode;

6, 7, 29, 43: Thin gate insulating film;

10, 24, 32, 34, 42: Photoresist film;

15, 21: Thin laminated gate insulating film;

15a, 21a: Thin anti-oxidation film:

16, 26: High dielectric constant film;

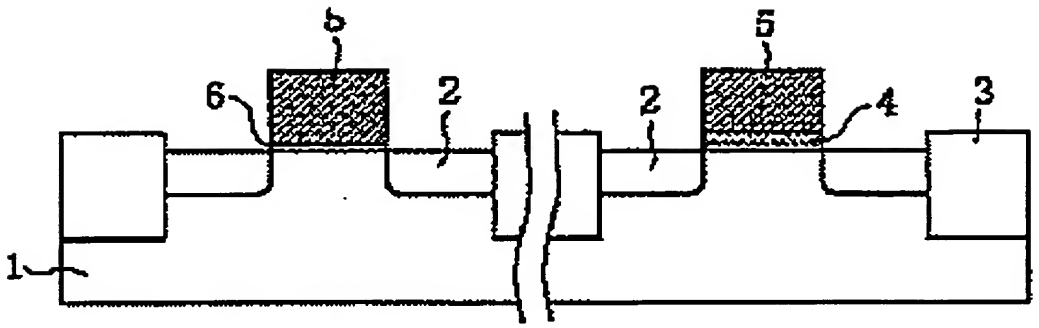
20, 25: Thick laminated gate insulating film;

20a, 25a: Thick laminated gate insulating film;

33, 39: Gate insulating film;

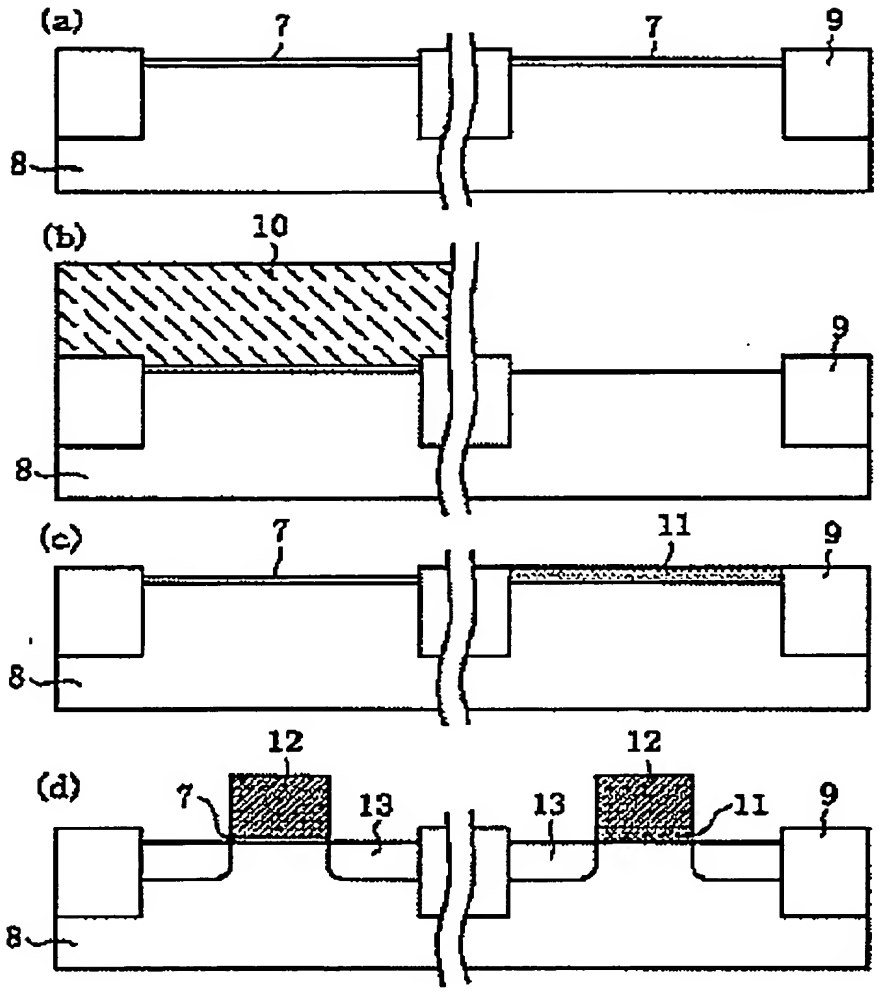
36: Gate insulating film of intermediate thickness.

FIG. 1



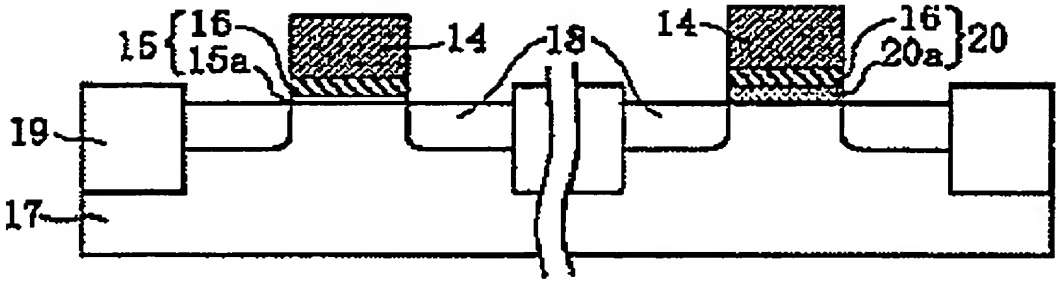
1: WELL
2: SOURCE AND DRAIN REGION
3: ELEMENT ISOLATING AND INSULATING FILM
4: THICK GATE INSULATING FILM
5: GATE ELECTRODE
6: THIN GATE INSULATING FILM

FIG. 2



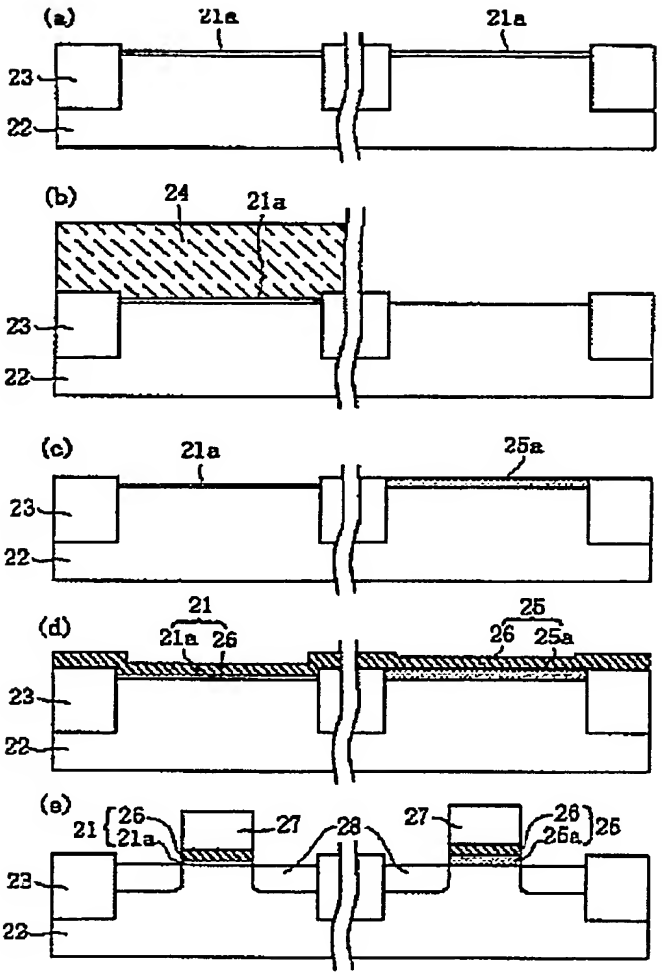
7: THIN GATE INSULATING FILM
8: WELL
9: ELEMENT ISOLATING AND INSULATING FILM
10: PHOTORESIST FILM
11: THICK GATE INSULATING FILM
12: GATE ELECTRODE
13: SOURCE AND DRAIN REGION

FIG. 3



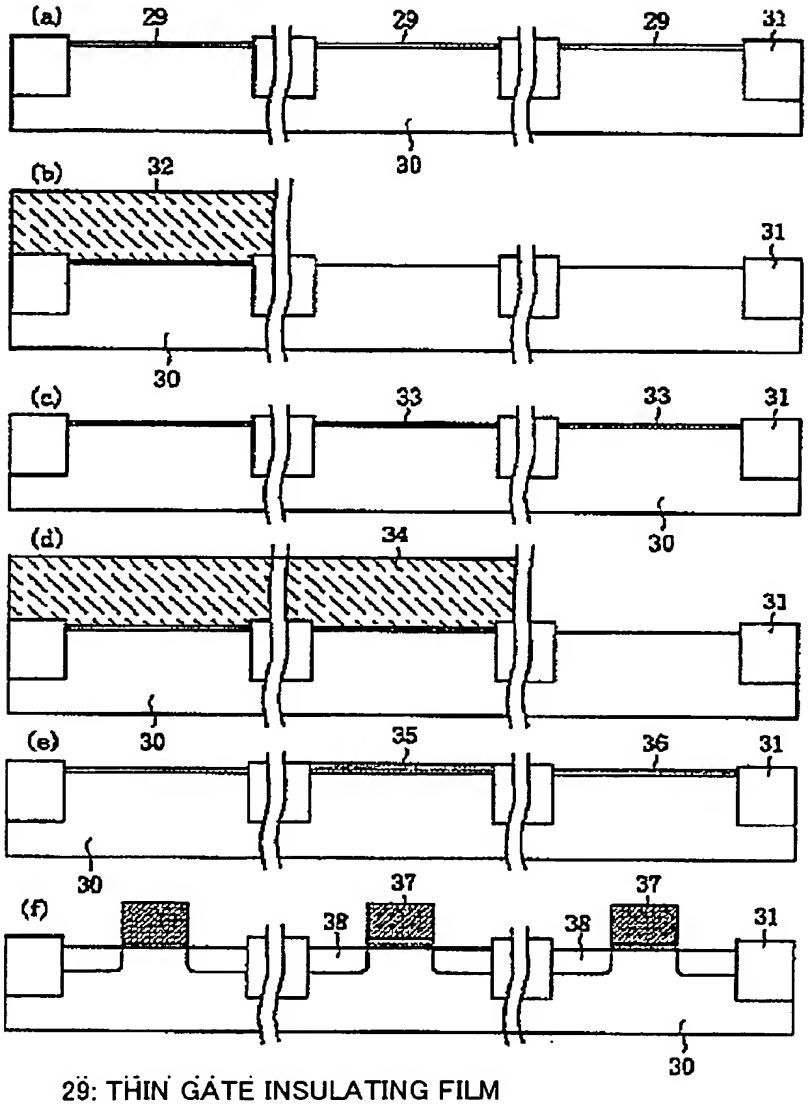
14: GATE ELECTRODE
15: THIN LAMINATED GATE INSULATING FILM
15a: THIN ANTI-OXIDATION FILM
16: HIGH DIELECTRIC CONSTANT FILM
17: WELL
18: SOURCE AND DRAIN REGION
19: ELEMENT ISOLATING AND INSULATING FILM
20: THICK LAMINATED GATE INSULATING FILM
20a: THICK LAMINATED GATE INSULATING FILM

FIG. 4



21: THIN LAMINATED GATE INSULATING FILM
21a: THIN ANTI-OXIDATION FILM
22: WELL
23: ELEMENT ISOLATING AND INSULATING FILM
24: PHOTORESIST FILM
25: THICK LAMINATED GATE INSULATING FILM
25a: THICK LAMINATED GATE INSULATING FILM
26: HIGH DIELECTRIC CONSTANT FILM
27: GATE ELECTRODE
28: SOURCE AND DRAIN REGION

FIG. 5



29: THIN GATE INSULATING FILM

30: WELL

31: ELEMENT ISOLATING AND INSULATING FILM

32, 34: PHOTORESIST FILM

33: GATE INSULATING FILM

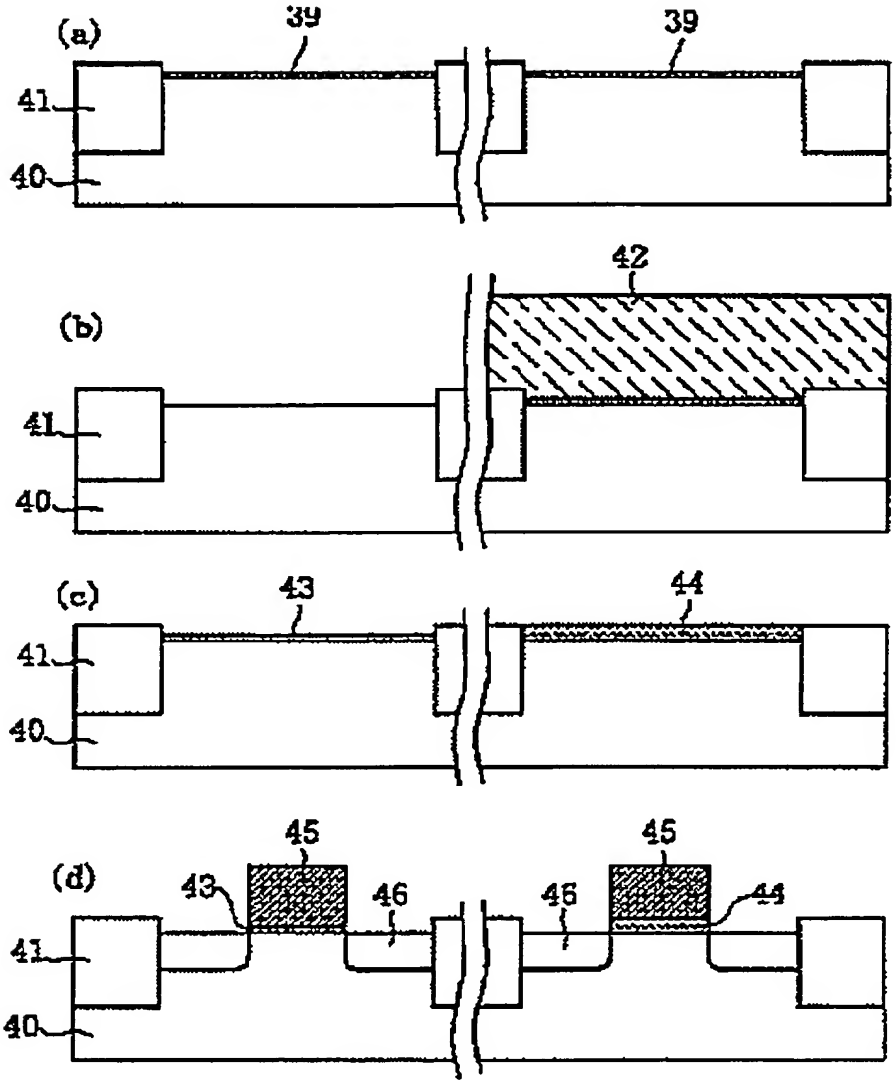
35: THICK GATE INSULATING FILM

36: GATE INSULATING FILM OF INTERMEDIATE THICKNESS

37: GATE ELECTRODE

38: SOURCE AND DRAIN REGION

FIG. 6



39: GATE INSULATING FILM
40: WELL
41: ELEMENT ISOLATING AND INSULATING FILM
42: PHOTORESIST FILM
43: THIN GATE INSULATING FILM
44: THICK GATE INSULATING FILM
45: GATE ELECTRODE
46: SOURCE AND DRAIN REGION